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# Logic based on magnetic tunnel junctions

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**Abstract**

Logic gate arrays are electronic devices delivering an output voltage which is a function of one, two or more input voltages. Usually, such circuits are made from CMOS subdevices (transistors) which provide an output function defined by the layout of the device. Thus such logic gate arrays are not programmable after the production and, moreover, they are volatile because inputs and output lose the information after power shutdown. Here, we describe the use of magnetic tunnel junctions for the preparation of alternative logic gate arrays. These devices are nonvolatile, i.e. keep the inputs and output after power shutdown, and they are field programmable, i.e. the output function can be defined even 'on the fly' during the operation. Potential drawbacks such as scalability and reproducibility will be addressed and possible solutions for these problems will be discussed.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

Magnetoresistive devices [1–3] already find their applications as sensors for a magnetic field, for example, for measurements of rotation angles or read heads in hard disk drives. Moreover, the research also focuses on their use in biosensors within lab-on-chip systems [4, 5]. The most important project is the development of the magnetoresistive random access memory [6, 7] (MRAM). Several large providers of RAM circuits are currently testing the potential benefits of these magnetic devices such as nonvolatile data storage, high speed for both reading and writing, a large number of operation cycles and good scalability down to the deep submicron level. Because this MRAM does not need the refresh cycles necessary for volatile memories, the number of read/write cycles for computing purposes could be increased dramatically compared to conventional RAM circuits.

A relatively new development as compared with MRAM or sensors is the use of magnetoresistive devices in logic circuits [8–10]. The realization of a logic based on the same principles and technologies as the—potentially universal—memory MRAM is of large interest, because it opens the way to a common technology platform for both storing as well

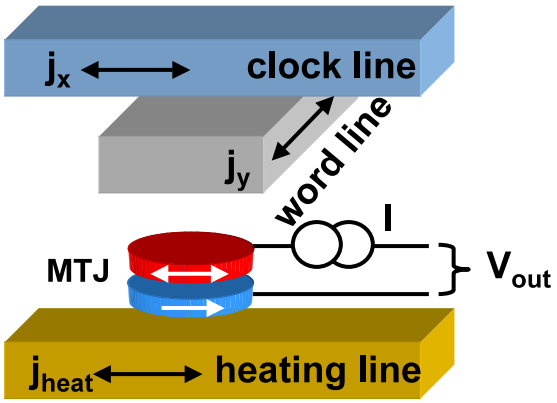


**Figure 1.** The simplest logic gate consisting of only one tunnelling cell (MTJ). The inputs are the clockline and the wordline, and optionally a current-carrying line heating the cell. The output is the voltage drop across the MTJ.

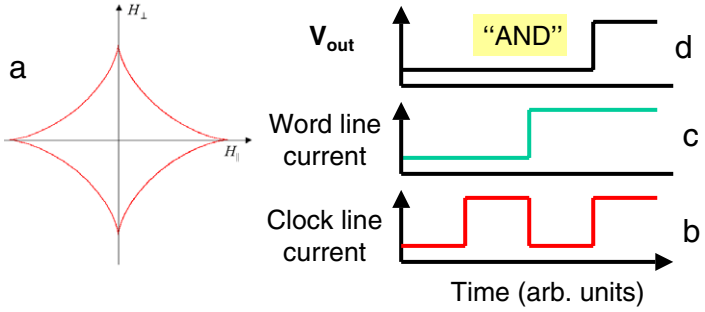


**Figure 2.** The operation principle of the gate shown in figure 1(a) The Stoner astroid of a idealized soft layer relevant for the switching with two perpendicular field pulses from the clockline and the wordline. (b) and (c) The time dependence of the currents on the clockline and the wordline, respectively, and (d) the output voltage $V_{out}$ if only the combination of clockline and wordline field can switch the magnetization.

as computing data. Moreover, magnetic logic gate arrays can be field programmable, leading to field-programmable logic gate arrays (FPGAs). Such FPGAs are programmable 'on the fly' and thus open also a path to fast reconfigurable computing [11].

Generally, the concept of using magnetic tunnel junctions (MTJs) for logic operations can be visualized as shown in figure 1: a current flowing through one (or more) magnetic tunnel junction(s) causes a voltage drop $V_{out}$. Because the resistance of the MTJ depends on the relative orientations of the magnetizations of the upper and lower electrode, this $V_{out}$ will change when one of the electrodes switches its magnetization (indicated by the double arrow in figure 1). Switching of the magnetization can be accomplished by several outer means. The most simple is driving current through wires (wordline and clockline in figure 1) close to the MTJ. These currents create a magnetic field which can switch the magnetization of the MTJ's soft electrode. Other possibilities are heating the MTJ so that also the hard electrode can be switched magnetically.

A scheme of operation of this simplest logic gate with only one MTJ is shown in figure 2: because the switching condition of the magnetization of the soft layer is given approximately by

the Stoner astroid (figure 2(a)), only the presence of both currents on the clockline and wordline (figures 2(b) and (c)) causes switching if appropriate values for the currents are chosen. Thus the output voltage $V_{out}$ (figure 2(d)) will change only if both currents are present. If the MTJ is switched by this procedure into the high resistive state (antiparallel magnetizations), then $V_{out}$ represents the logic 'AND' relation between the clock-current and the word-current. In the reversed case of switching from the high to the low resistive state, the function is 'NAND'. Thus, in this simplest version, already two functions can be realized; by using the clockline current also, clocked operation of this circuit is possible.

Suggestions for using magnetoresistive devices in logic circuits were made back in the early 1960s, when ferrite cores were used to store and process information [12].

In 2000, Black and Das [8] suggested using magnetic devices showing spin-dependent transport for a programmable logic. This concept was further elaborated by several groups especially with MTJs as core devices. Prinz [3] showed that logic could be one part of a complete scheme of magnetoelectronics. Richter *et al* [9] experimentally demonstrated a field-programmable logic gate consisting of four MTJs. Ney *et al* [10] discussed a concept, where only one tunnelling junction can form a programmable logic gate, if it is possible to also switch the hard (fixed) magnetic electrode. This could be accomplished by, for example, using the heating line sketched in figure 1.

Here, we concentrate on the first approach using a bridge-type circuit consisting of four tunnelling junctions.

## 2. Experimental details

### *2.1. The basic film stacks for MTJ devices*

In the MTJs used for logic, the basic film stacks consist of a seed and conduction layer, a natural antiferromagnet for pinning the hard magnetic electrode and a single ferromagnetic layer forming one tunnelling electrode or an artificial antiferromagnet, i.e. a trilayer system ferromagnet/nonmagnet/ferromagnet which is coupled antiferromagnetically by indirect exchange coupling [13]. On this electrode, the tunnelling barrier consisting of either $Al_2O_3$ or MgO is prepared. This is one of the most crucial preparation steps for forming MTJs because the resistance depends exponentially on the thickness of the insulator, and the tunnelling magnetoresistance (TMR) is critically affected by the properties of the insulator and the interfaces.

After having prepared the barrier, the subsequent layers of upper electrode, conductor and protection layer are deposited. The preparation was done in a commercial sputtering system (Leybold CLAB) with 4 inch targets and oxidized Si(100) substrates with around 100 nm $SiO_2$. Generally, the layers are rather thin (between 1 nm and 20 nm), so the settings for the sputtering power as well as for the Ar pressure were as low as possible. After preparation, the film system was annealed and field cooled for one hour in a magnetic field of 1000 Oe and at a maximum temperature of 275 °C for initiating the exchange bias between the natural antiferromagnet and the ferromagnetic (hard) electrode.

In figure 3, we show the signal of the magnetooptical Kerr effect of a system $Ta^{6.5}/Cu^{30}/Ta^{19}/Cu^{8.2}/Mn_{83}Ir_{17}{}^{10.6}/Co_{70}Fe_{30}{}^{2.3}/Al_2O_3{}^{1.5}/Ni_{80}Fe_{20}{}^{4}/Ta^{5}$, where the indices give the composition (lower index) and the thicknesses in nm (upper index).

As can be seen in figure 3, the preparation procedure results in two magnetically well separated electrodes. The exchange biasing of the hard electrode amounts to about 1300 Oe, so that a well defined plateau is formed between the magnetic switching of the soft (upper) and the hard (lower) electrode.

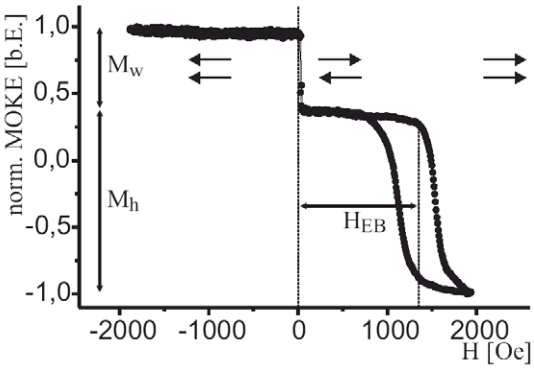


**Figure 3.** The normalized signal from the magnetooptical Kerr effect of the MTJ stack described in the text. The hysteresis at small field stems from the soft magnetic electrode, whereas the loop from the hard electrode is shifted by 1300 Oe due to the exchange biasing with IrMn.

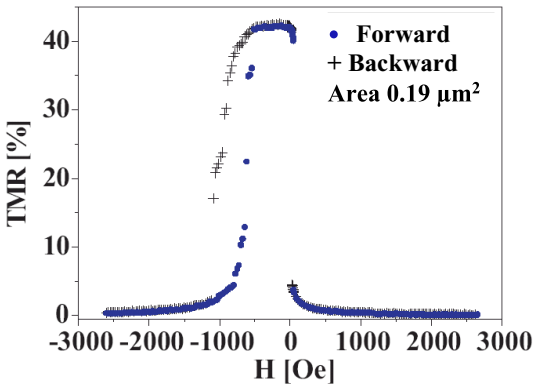


**Figure 4.** The TMR major loop, i.e. the dependence of the resistance of an MTJ on the external field corresponding to the MOKE curve of figure 3. The amplitude of the TMR is defined as $\Delta R/R_{\mathrm{L}}$.

This can be also seen on the TMR loop of this system shown in figure 4. Here, we present a major loop, i.e. the field range is so large, that both electrodes are switched. The TMR effect amplitude in this standard system amounts to around 42% resistance change upon magnetization switching (note that the TMR is defined here as $(R_{\mathrm{H}} - R_{\mathrm{L}})/R_{\mathrm{L}}$). This is a typical value found for the combination of the ferromagnets $Co_{70}Fe_{30}$ and $Ni_{80}Fe_{20}$ in tunnelling cells with an $Al_2O_3$ barrier.

After the preparation of this basic film stack, additional insulators and conducting films are deposited in order to create the wordlines and clocklines as sketched already in figure 1. For small tunnelling junctions in the range below 300 nm, we used instead of the single $Co_{70}Fe_{30}{}^{2.3}$ hard electrode an artificial antiferromagnet $Co_{75}Fe_{25}{}^{3}/Ru^{0.9}/Co_{75}Fe_{25}{}^{2.8}$. This reduces drastically the stray field of the hard layer which leads to a shift of the soft layer's hysteresis.

### *2.2. Preparation of logic gate arrays*

The preparation of sub-$\mu$m logic gates with four MTJs as shown in figure 5 requires a series of relatively sophisticated e-beam processes [13]. First, the MTJs are patterned followed by

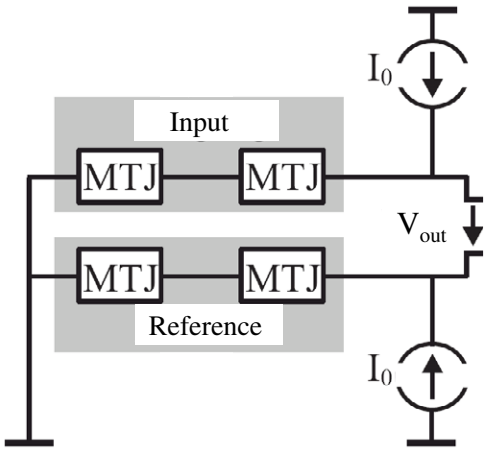


**Figure 5.** Schematic circuit of a field-programmable logic gate array consisting of two input MTJs and two reference MTJs. The value of the current driven through all MTJs is $I_o$, as shown. The output $V_{\text{out}}$ is the voltage difference between the input and the reference chain.

the preparation of the upper contact lines of the MTJs. Then, the clocklines and wordlines are prepared with insulating 100 nm thick $SiO_2$ separating both the contact lines of the MTJs as well as the clockline and wordline. After that, the complete structure is covered by a $TaO_X$ protection layer (5 nm). The chips with four nominally identical logic gates are then cut and wire bonded in a conventional chip socket. In our layout, each MTJ can be also characterized individually in order to evaluate variations of the resistance and the TMR within one gate.

Examples for the result of this procedure are shown in figures 6(a) and (b): a complete logic gate consisting of four electrically connected MTJs as already shown in figure 5 (figure 6(a)) and one individual tunnelling cell with a size of about 200 nm × 100 nm (figure 6(b)). Provided all lithography steps are successfully done, the properties of the MTJs do not change with respect to their expected resistance and TMR within the margins found already on extended samples.

## 3. Properties of the logic gates

### *3.1. Programmed logic operations—proof of principle*

For the logic operations, current pulses are passed through the wordlines on two of the MTJs, which create a magnetic field able to switch the soft electrode of two MTJs connected in series. In figure 7, we show the resulting resistance of this chain as a function of the applied current pulses in the two wordlines ($I_{\text{W1}}$ and $I_{\text{W2}}$ in figure 6(a), respectively). The resistance changes according to the switching of the individual MTJs soft layers between a maximal value with both MTJs being in the high resistive state $R_{\text{H}}$ to a mixed state ($R_{\text{H}}/R_{\text{L}}$), the minimum resistance value ($R_{\text{L}}/R_{\text{L}}$), the next mixed state ($R_{\text{L}}/R_{\text{H}}$) and then back to the original state ($R_{\text{H}}/R_{\text{H}}$). If one identifies resistance values smaller than, in this case, 320 kΩ with logic 0 and larger than 340 kΩ with logic 1, then this corresponds to an 'AND' function relating the two (wordline) inputs. This would be then the non-programmable operation of only two MTJs. For programming the function, the two other MTJs (connected also in series) are necessary.

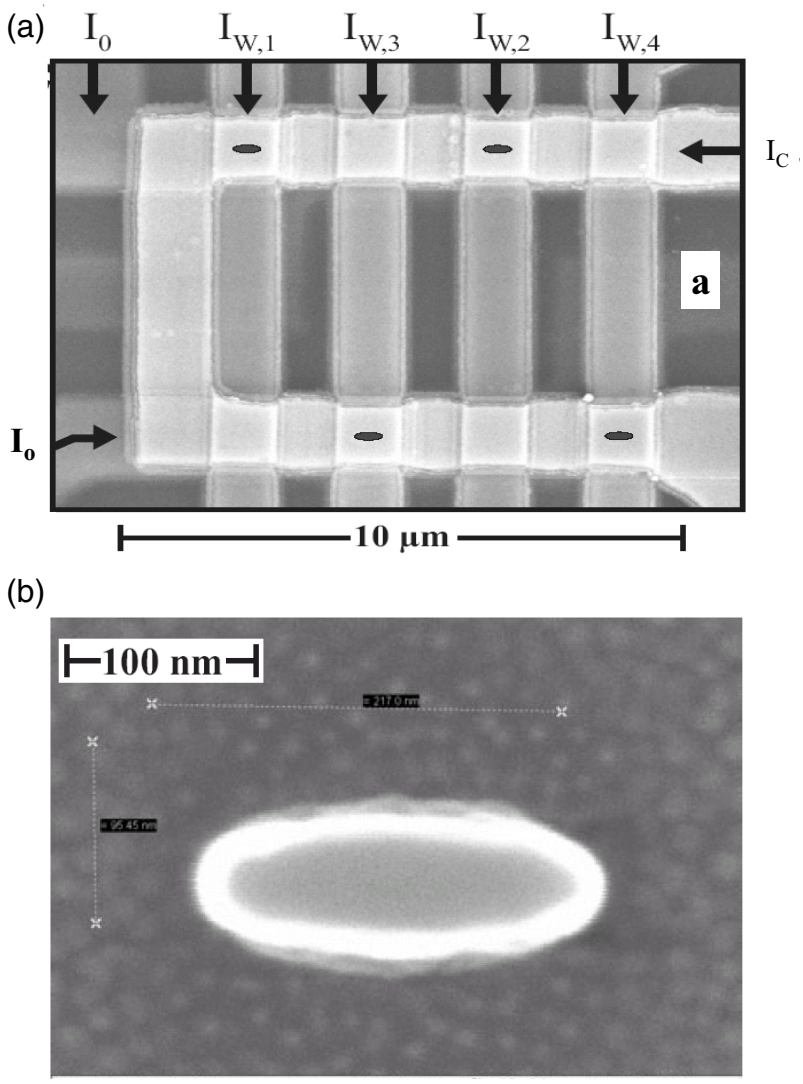


**Figure 6.** (a) SEM image of a complete field-programmable logic gate made by several subsequent e-beam lithography steps. The locations of the (buried) magnetic tunnel junctions are indicated by black ellipses. $I_o$ is the value of the current running through the upper (input) and the lower (reference) MTJs. $I_c$ is the common clock-current and $I_{W1-4}$ are the word-currents for switching the MTJs. (b) SEM image of the smallest single tunnel junction employed in the FPGAs. The shape is elliptic, about 200 nm × 100 nm.

This mode of operation (as sketched in figure 5) is demonstrated in figure 8: here two functions (NAND and NOR) have been implemented by setting the two reference MTJs in figure 5 to the states $(R_L/R_L)$ for the NAND function and $(R_L/R_H)$ for the NOR.

As can be seen from figure 8, the programming action changes the output of the logic gate array from one Boolean function to another. Because the programming action consists of magnetically switching the soft electrode of one of the reference MTJs, this is as fast as transferring the input from the current pulses to the resistance state of the input MTJs.

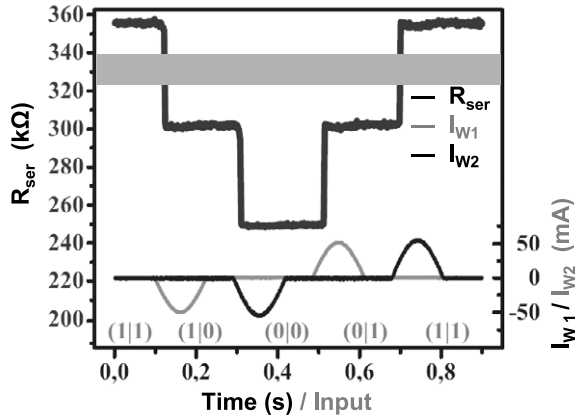


**Figure 7.** Resistance of the series of two (input) MTJs upon switching. Here, hard switching was employed, i.e. the two word-currents $I_{W1,2}$ shown in the lower part were chosen large enough for switching the MTJs without clock-current. The resistance takes the distinct values corresponding to the states $R_H/R_H$, $R_H/R_L$, $R_L/R_L$ and $R_H/R_L$ of the MTJs.

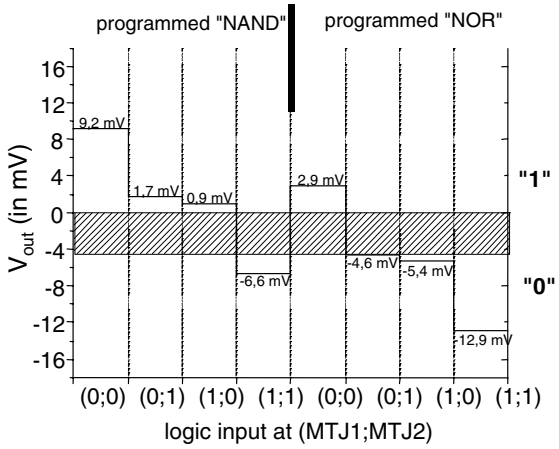


**Figure 8.** Output voltage $V_{out}$ of a complete FPGA (compare figure 5) upon changing the reference MTJs from the state $R_L/R_L$ to $R_L/R_H$ corresponding to a programmed 'NAND' and 'NOR', respectively. The function is verified by switching the input MTJs with appropriate word-currents and clock-currents. The shaded area marks the gap necessary between $V_{out}$ corresponding to logic 1 and 0. Note that in this case the gap amounts to only 5 mV.

Moreover, the state of the logic gate array (i.e. inputs and output) are stored in a nonvolatile manner in the MTJs.

### *3.2. Scalability*

One major precondition for the applicability of this concept for logic devices is the scalability of the field-programmable logic gate arrays down to sizes common for microelectronic devices (100 nm range) while simultaneously maintaining operability, i.e. reasonable magnetic switching properties as well as homogeneous resistance and TMR.

As already shown in figure 6(b), working tunnelling cells with an area of 0.02 $\mu m^2$ have been realized [13]. The requirements for logic, however, are more stringent than for

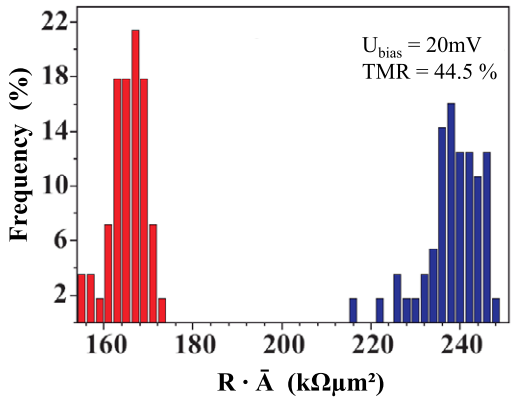


**Figure 9.** Probability distribution of the high and low resistive states (area–resistance product) of a large number of tunnelling cells. The shapes are close to Gaussian distributions. In this case, the variances are around 4% in both cases, allowing for a distinct region between the two distributions.

**Table 1.** Standard deviations of several physical properties of the investigated magnetic tunnel junctions.

| Property | Standard deviation (%) |
|---|---|
| Size | 6.9 |
| Low resistance $R_L$ | 5.5 |
| Area resistance product | 6.4 |
| TMR from magnetic switching | 2.1 |
| TMR from rotation measurements | 1.9 |

storing devices like MRAMs. Because, in the proposed layout, four MTJs are compared, their resistance and TMR values must be equal within a very small tolerance. Because the area of sub-100 nm patterns generated lithographically varies by already 5% (depending on, for example, the quality of the e-beam lithography machine and the resists), the accuracy for the electronic and magnetic properties of the MTJs themselves must be as good as possible.

In figure 9, we show the results for the variances of the resistance for the tunnelling cells with $Al_2O_3$ barriers in the low and high resistive state, respectively [14]. In table 1, we summarize results obtained for a variety of properties averaged over a large number of tunnelling cells. All variances are in the range 5%–7%, where in our case the lithography accounts for roughly 5% of the deviations. For completeness, we also included values for the TMR measured by rotating the magnetization of the soft magnetic electrode. These values are usually slightly larger than those found by just switching the magnetization between nominally parallel and antiparallel states. In accordance with previous findings, this points to a slight 'ripple' in the exchange pinning direction of the hard magnetic electrode, which in this case amounts to about $\pm 2^\circ$.

In summary, the scalability seems to be guaranteed with respect to the MTJs themselves, but a variation of the properties in the range of $\pm 5\%$ seems to be unavoidable if the sub-100 nm range is entered.

For the scalability, the most crucial point is the current needed in the clocklines and wordlines for switching the magnetizations. These currents amount to some milliamperes, and they do not scale down when the MTJs are made smaller. Thus the width of these lines must be around 1 $\mu$m, which severely hinders downscaling of the complete logic gate arrays.

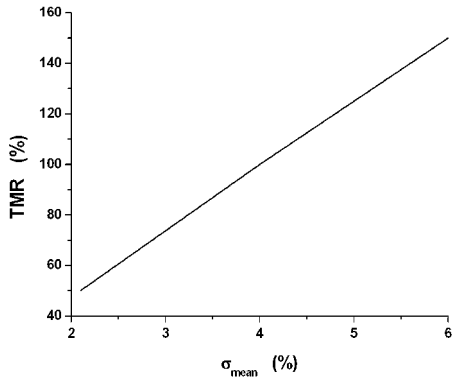


**Figure 10.** The minimum TMR effect amplitude for a reliable high-yield production of working FPGAs with a 4-$\sigma$ criterion (i.e. $Y = 4$ in equation (2)). The area below the curve leads to intolerably large numbers of FPGAs with too much overlap between the output voltage states corresponding to logic 1 and 0.

### *3.3. Criteria for variances in magnetic FPGAs*

As already mentioned in section 3.1, a gap between the output states of $V_{\text{out}}$ is necessary in order to enable the electronics subsequent to the logic gate array to distinguish unambiguously between $V_{\text{out}}$ being logic 0 or logic 1. Usually this gap should not be smaller than about 30 mV in order to avoid problems related with the signal to noise ratio. If we consider the worst case, i.e. if all variances are added according to Gaussian error propagation and the gate (figure 6(a)) is switched from all four MTJs being in the high resistive state to only one of them being at $R_{\text{L}}$, then variances of $V^1_{\text{out}}$ ($\sigma_1$) corresponding to logic 1 and $V^2_{\text{out}}$ ($\sigma_2$) will be

$$\begin{aligned} \sigma_1 &= I \cdot \sqrt{4\sigma_{\text{R}} + 4\sigma_{\text{TMR}}} \\ \sigma_2 &= I \cdot \sqrt{4\sigma_{\text{R}} + 3\sigma_{\text{TMR}}}, \end{aligned} \tag{1}$$

where $I$ is the current driven through the MTJs and $\sigma_{\text{R}}$ and $\sigma_{\text{TMR}}$ are the variances of the low resistive state and the TMR, respectively.

Evaluating the yield of working MTJs with realistic values is then possible. By calculating the gap between $V^1_{\text{out}}$ and $V^2_{\text{out}}$, one can find the minimum required resistance increase $\Delta R$ necessary for obtaining this gap.

$$\Delta R \cdot I > 30\,\text{mV} + Y \cdot I \cdot (\sigma_1 + \sigma_2). \tag{2}$$

Equation (2) means that there is a minimum of the gap which amounts to 30 mV plus a reliability factor $Y$ (usually set to 4) times the variances of the low plus those of the high resistive states.

Taking typical values for our MTJs, this results in the dependence of the minimum required TMR to fulfil this criterion as a function of the mean standard deviation (i.e. the mean value of $\sigma_1$ and $\sigma_1$, respectively) shown in figure 10. According to these results, a TMR of around 50% is not enough to guarantee a high yield production of working logic gate arrays with MTJs because, for this TMR, standard deviations of only 2% would be necessary [14]. An increase of the TMR to around 100%, however, changes the situation drastically, because then, around 4% standard deviation would be possible, which should be within reach for a professional Si chip production facility.

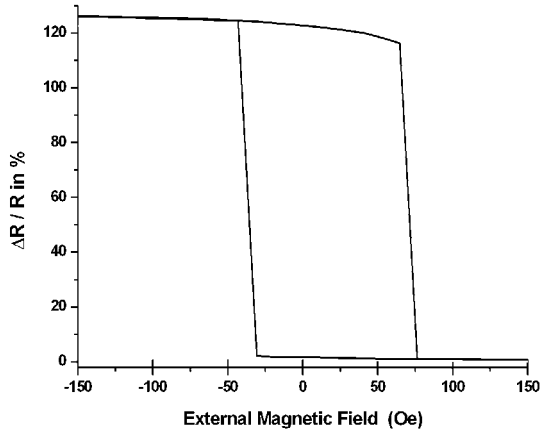


**Figure 11.** A TMR minor loop of a tunnel junction with MgO barrier (1.5 nm thick) and CoFeB electrodes. The area resistance product of these junctions is as small as 6.5 Ω $\mu$m$^2$ in the low-resistive state ($R_L$). The TMR in this example is 126%. Thus variances of around 5% could be tolerated for a high-yield production of FPGAs (see figure 10).

## 4. Perspectives for magnetic logic

In the last section, we have identified some major obstacles for a further development of magnetic logic:

- The TMR ratio of around 50% obtained for standard $Al_2O_3$-based MTJs might be enough to prepare some working FPGAs in the laboratory, but it does not satisfy the needs of a high-yield production.
- The currents in the clocklines and wordlines needed to switch the tunnelling cells are too large and do not scale down with the size of the MTJs.

Concerning the first point, major advances have been made in recent time due to applying MgO as new barrier material [15, 16]. TMR values of more than 300% have been reported at room temperature, which would completely relax the requirements for the standard deviations of resistance and TMR in FPGAs. Because, however, the solution for the second obstacle could be current-induced magnetization switching [17, 18] (CIMS), the area–resistance product of the barrier must not exceed around 50 Ω $\mu$m$^2$, because only then can enough current be pressed through the MTJ without destroying it. We have therefore tried to prepare low-resistive MgO-based tunnelling elements. In figure 11, we show a typical minor loop for this structure.

Here, the area resistance product is 6.5 Ω $\mu$m$^2$ allowing for current density of up to around $1.3 \times 10^7$ A cm$^{-2}$. Nevertheless, the TMR is around 126%, i.e. well above the threshold of 100% for a reliable production.

For these junctions, we carried out CIMS experiments, i.e. the voltage across the MTJ was pulsed to a certain value and then the resistance was measured at a low voltage of 20 mV. The result of this attempt is shown in figure 12, where the applied voltage pulse was already replaced by the corresponding value of the current density.

Pulsing a current density between $8 \times 10^6$ and $13 \times 10^6$ A cm$^{-2}$ through these MTJs leads to switching back and forth the magnetization of the soft layer between parallel and antiparallel alignment, respectively.

Because this switching current in CIMS scales down in parallel with the area of the tunnelling junctions, these MgO-based tunnel junctions seem to be the ideal candidates

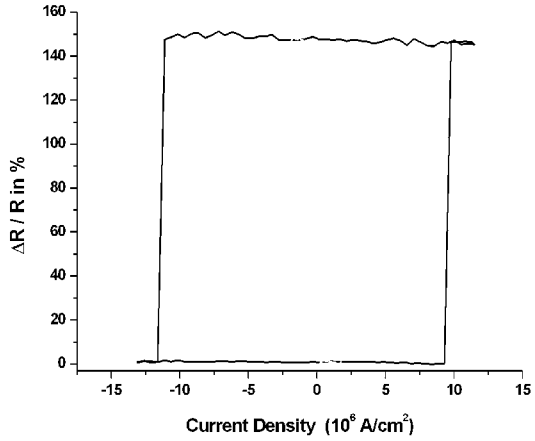


**Figure 12.** A minor loop of the tunnel junction from figure 11 taken by current-induced switching. Here, a current pulse was applied to the junction and the resistance was subsequently determined at low bias voltage (20 mV). The junction switches from $R_L$ to $R_H$ (antiparallel state) at $9 \times 10^6$ A cm$^{-2}$ and back to $R_L$ at $13 \times 10^6$ A cm$^{-2}$.

for the realization of working and economically producible field-programmable logic gate arrays.

## 5. Summary

In this paper, we have presented investigations of the potential of magnetic tunnel junctions for the realization of a magnetic logic which is nonvolatile, fast and reprogrammable 'on the fly'. Using conventional $Al_2O_3$-based tunnel junctions, we have given a proof of the principle of this type of logic gate array with four tunnelling cells, two of them used as input and two of them building the reference. For really introducing this principle into new electronic (magnetic) devices, we identified several obstacles. First, the TMR amplitude should be at least around 100% in order to enable a production of such FPGAs with a reasonable yield. Second, the currents needed for the magnetization switching turns out to be too large and not downscalable, thus hindering a cost-effective layout.

Using the new development of low-resistive MTJs with MgO barriers and a TMR considerably larger than 100%, we have demonstrated that these tunnel junctions could considerably improve the perspectives of magnetic logic for industrial applications. In fact, these new devices solve the two main problems identified for the conventional $Al_2O_3$-based systems.

Due to their high-temperature stability, they could also open a way to switch the hard magnetic layer by thermally changing the exchange bias direction. Moreover, for Heusler materials as magnetic electrodes [19], it was found that a change of the sign of the TMR can be found if the bias voltage is changed from low to high values [20]. Thus, using these effects as new ways for changing the functions of the FPGAs, new degrees of freedom can be introduced which can be used to further increase their variability.

## Acknowledgments

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## References

[1] Moodera J S, Kinder L R, Wong T M and Meservey R 1995 *Phys. Rev. Lett.* **74** 3273
[2] Miyazaki T and Tezuka N 1995 *J. Magn. Magn. Mater.* **139** 231
[3] Prinz G A 1998 *Science* **282** 1660
[4] Baselt D R, Lee G U, Natesan M, Metzger S W, Sheehan P E and Colton R J 1998 *Biosens. Bioelectron.* **13** 731
[5] Brzeska M, Panhorst M, Kamp P B, Schotter J, Reiss G, Pühler A, Becker A and Brückl H 2004 *J. Biotechnol.* **112** 25–33
[6] Gallagher W J and Parkin S S P 2006 *IBM J. Res. Dev.* **50** 5
[7] Motoyoshi M and Kano H 2005 Ways of achieving high-performance MRAMs *IEEE VLSI-TSA Int. Symp. on VLSI Technology* p 82
[8] Black W C Jr and Das B 2000 *J. Appl. Phys.* **87** 6674
[9] Richter R, Bär L, Wecker J and Reiss G 2002 *Appl. Phys. Lett.* **80** 1291
[10] Ney A, Pampuch C, Koch R and Ploog K H 2002 *Nature* **418** 509
[11] Hartenstein R and Grünbacher H (ed) 2000 The roadmap to reconfigurable computing *Proc. FPL2000 (Aug. 2000)* (*LNCS*) (Berlin: Springer)
[12] Gianola U F 1961 *J. Appl. Phys.* **32** 27
[13] Meyners D, Rott K, Brückl H, Reiss G and Wecker J 2006 *J. Appl. Phys.* **99** 023907
[14] Reiss G and Meyners D 2006 *Appl. Phys. Lett.* **88** 043505
[15] Parkin S S P, Kaiser C, Panchula A, Rice P M, Hughes B, Samant M and Yang S H 2004 *Nat. Mater.* **3** 862
[16] Yuasa S, Nagahama T, Fukushima A, Suzuki Y and Ando K 2004 *Nat. Mater.* **3** 868
[17] Slonczewski J C 1996 *J. Magn. Magn. Mater.* **159** L1
[18] Diao Z T, Pakala M, Panchula A, Ding Y F, Apalkov D, Wang L C, Chen E and Huai Y M 2006 *J. Appl. Phys.* **99** 08G510
[19] Schmalhorst J, Kämmerer S, Reiss G and Hütten A 2005 *Appl. Phys. Lett.* **86** 052501
[20] Thomas A, Meyners D, Ebke D, Liu N-N, Sacher M D, Schmalhorst J, Reiss G, Ebert H and Hütten A 2006 *Appl. Phys. Lett.* **89** 012502